IN THE CLAIMS

1. (Currently Amended) A digital microelectronic circuit comprising a clocked data-processing unit ~~(1)~~ and a converting unit ~~(2)~~ which reads in data present at the output of the data-processing unit, performs a predetermined converting operation on the data and passes on the converted data, characterized in that the converting unit is realized in an asynchronous logic circuit, such that the period of time for performing the converting operation is shorter than the shortest time interval to the next change of the data present at the output of the data-processing unit.

2. (Currently Amended) ~~A~~ **The** digital microelectronic circuit as claimed in claim 1, characterized in that the converting operation is an encryption, a compression, an error correction, a hash function and/or checking operation~~, preferably a CRC operation~~.

3. (New) The digital microelectronic circuit of Claim 1, wherein the converting operation is a CRC operation.

4. (New) The digital microelectronic circuit of Claim 1, wherein the converting unit passes on the converted data to the data-processing unit.

5. (New) The digital microelectronic circuit of Claim 1, wherein the converting unit is operable to receive data to be converted from a logic block other than the data-processing unit.

6. (New) A digital system, comprising:

a first synchronous data processing circuit that operates at a first clock rate that has a first clock period; and

an asynchronous converting unit, coupled to the first synchronous data processing circuit, the asynchronous converting unit having a conversion time that is less than the first clock period;

wherein the first synchronous data processing circuit is operable to provide digital data to the asynchronous converting unit such that the provided data does not change faster than the first clock period; and wherein the asynchronous converting unit is operable to provide converted digital data to the first synchronous data processing circuit.

7. (New) The digital system of Claim 6, wherein the asynchronous converting unit further comprises an input connection, that is not connected to the first synchronous data processing circuit, the input connection operable to receive digital data for conversion.

8. (New) The digital system of Claim 6, wherein the asynchronous converting unit further comprises an output connection, that is not connected to the first synchronous data processing circuit, the output connection operable to provide digital converted data.

9. (New) The digital system of Claim 6, wherein the asynchronous converting unit is operable to perform at least one of the tasks selected from the group consisting of encryption, compression, error correction, and hash functions.

10. (New) A method of processing data, comprising:

generating digital data in a synchronous data processing unit;

providing first digital data to an input of an asynchronous digital converting unit and holding the first digital data at the input;

asynchronously computing a digital result in the asynchronous digital converting unit; and

providing second digital data, subsequent to asynchronously computing the result, to the input of the asynchronous digital converting unit.

11. (New) The method of Claim 10, further comprising providing the asynchronously computed digital result to the synchronous data processing unit.